

IPPC1501-RE

User Manual

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Safety Information

Your IPPC1501-RE is designed and tested to meet the latest standards of safety for information technology equipment. However, to ensure your safety, it is important that you read the following safety instructions.

Setting up your system

- Read and follow all instructions in the documentation before you operate your system.
- Do not use this product near water.
- Set up the system on a stable surface. Do not secure the system on any unstable plane.
- Do not place this product on an unstable cart, stand, or table. The product may fall, causing serious damage to the product.
- Slots and openings on the chassis are for ventilation. Do not block or cover these openings. Make sure you leave plenty of space around the system for ventilation.
Never insert objects of any kind into the ventilation openings.
- This system should be operated from the type of power indicated on the marking label. If you are not sure of the type of power available, consult your dealer or local power company.
- Use this product in environments with ambient temperatures between -5°C and 50°C.
- If you use an extension cord, make sure that the total ampere rating of the devices plugged into the extension cord does not exceed its ampere rating.
- **DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C OR ABOVE 60° C. THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.**

Care during use

- Do not walk on the power cord or allow anything to rest on it.
- Do not spill water or any other liquids on your system.
- When the system is turned off, a small amount of electrical current still flows. Always unplug all power, and network cables from the power outlets before cleaning the system.
- If you encounter the following technical problems with the product, unplug the power cord and contact a qualified service technician or your retailer.
 - The power cord or plug is damaged.
 - Liquid has been spilled into the system.
 - The system does not function properly even if you follow the operating instructions.
 - The system was dropped or the cabinet is damaged.

Lithium-Ion Battery Warning

CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

NO DISASSEMBLY

The warranty does not apply to the products that have been disassembled by users

WARNING
HAZARDOUS MOVING PARTS
KEEP FINGERS AND OTHER BODY PARTS AWAY

Acknowledgments

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CHAPTER 1 INTRODUCTION

1.1 General Description

The IPPC1501-RE is a fanless design panel pc, powered by an Intel Atom processor D2550 with a speed of 1.86GHz. It supports one SO-DIMM slot that can accommodate up to 4GB DDRIII 1066MHz FSB memory. Some of the main features include 4x USB connector, 2x COM port, 1x SATA HDD space support and 12V~24V DC power input. It is ideal for industrial automation, and factory automation applications.



IPPC1501-RE front side view



IPPC1501-RE rear side view

1.2 System Specification

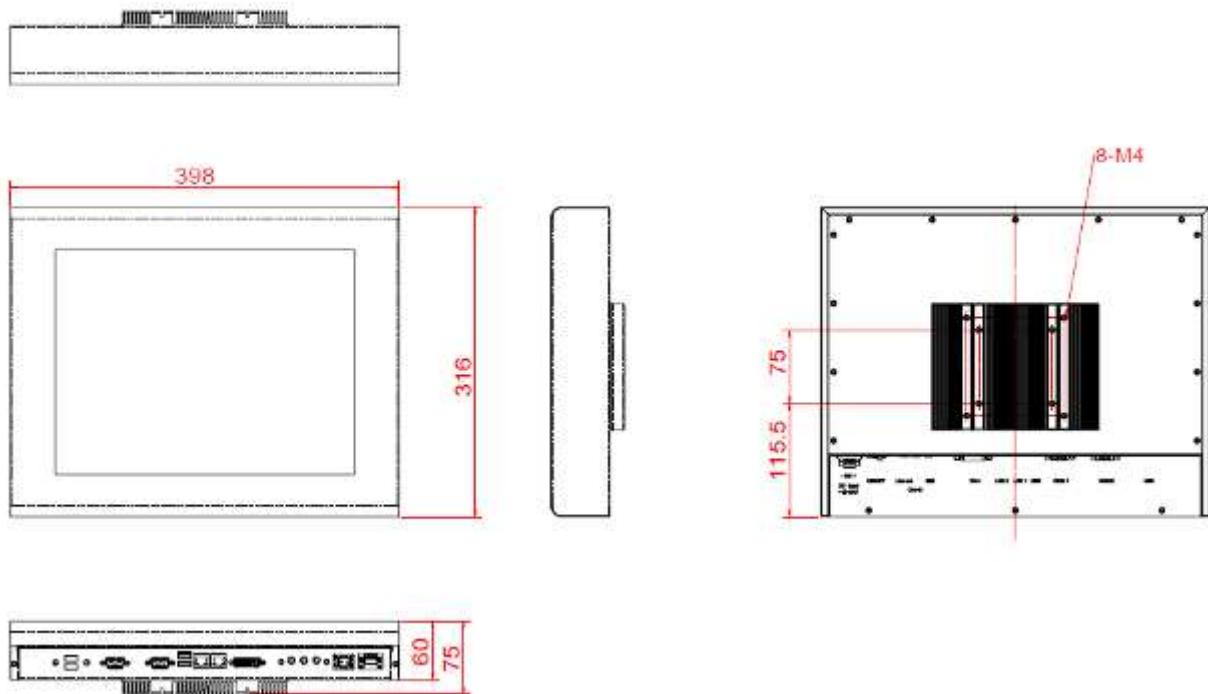
1.2.1 Hardware Specifications

Model Name	IPPC1501-RE
System Mainboard	IB895
CPU	Intel Atom Process D2550 1M Cache, 1.86GHz
Chipset	Intel NM10 Express Chipset
Memory	1 x DDR3 1333 SO-DIMM, maximum 4GB. Default 2GB
I/O Interface	1 x DVI-I 2 x 10/100/1000 Base-T LAN w/ RJ45 connector 4 x USB2.0 w/ type-A connector 1 x RS-232/422/485 (Default: RS-232) w/ DB9M connector 1 x RS-232 w/ DB9M connector 1 x 3 pin DC power terminal 1 x power rock switch (ATX)
Storage	1 x 2.5" SATA interface device bay, default 500GB
Expansion Slots	None
Power Supply	12V~24V DC-in, 60W power adaptor
LCD Size	15" TFT LCD
LCD Color	16.2M colors
LCD Resolution	1024 x 768
LCD Brightness	400 cd/m2
LCD Viewing Angle	160(H)/140(V)
Backlight MTBF	50,000 hrs
Touch Screen	Resistive Touch Screen
Construction	Black sheet metal
Mounting	VESA mount 75x75 and 100x100 mm
Dimensions (W)x(H)x(D) mm	398 x 316 x 75 mm
Operating Temperature	-5°C~ 50°C (23°F~140°F)
Storage Temperature	-20°C ~ 60°C (-4°F~176°F)
Relative Humidity	10~90% (non-condensing)
Protection Class	Front panel IP65

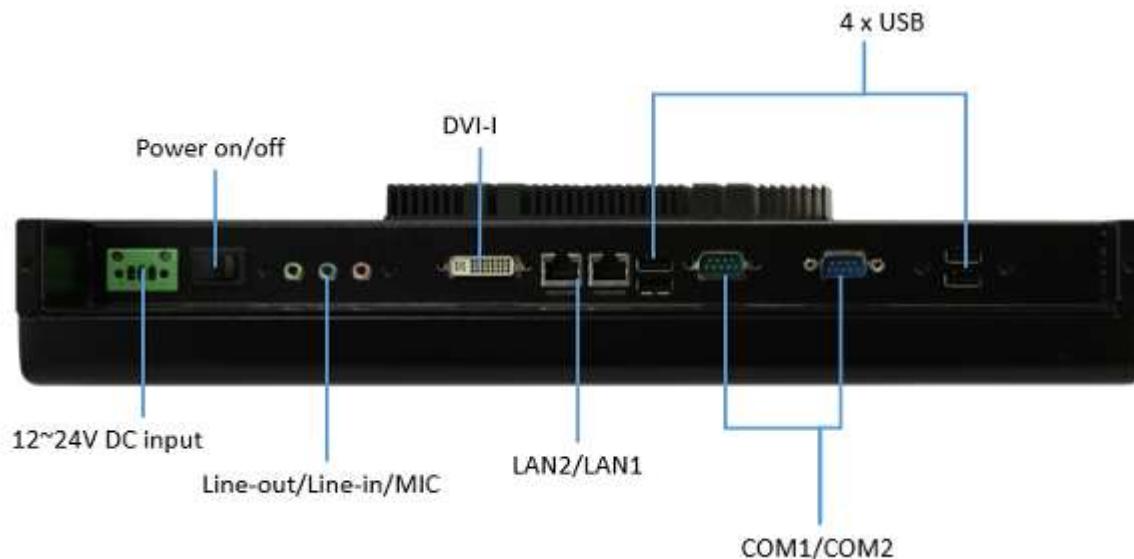
**This specification is subject to change without prior notice.*

1.2.2 Dimensions

IPPC1501-RE



1.2.3 I/O View

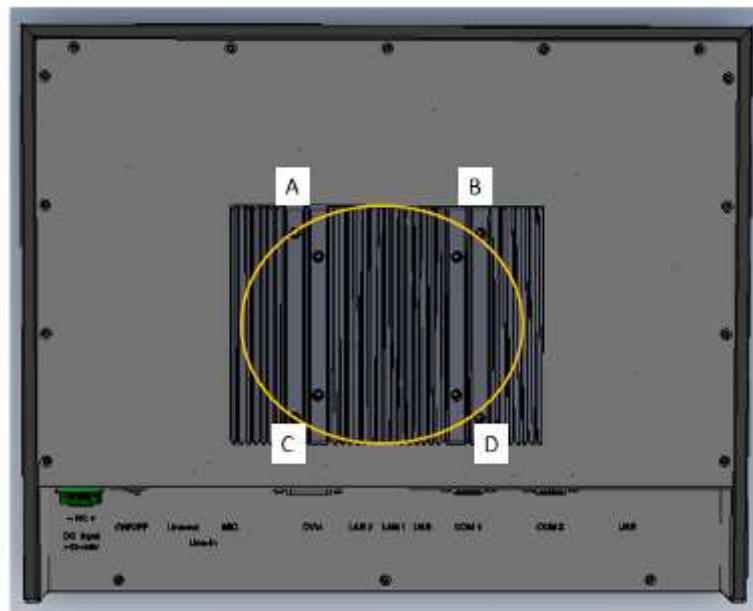


1.3 Packing List

Part No.	Description	Qty
1	Terminal block for power input	1 pc
2	Driver CD	1 pc

1.4 Installation

1.4.1 Installing the VESA Mount



1. The VESA mount holes are compatible with VESA standard - 75x75 and 100x100
2. Put your VESA mounting kit on the orange area as shown above.
3. Lock the screws from A to D.

CHAPTER 2 MOTHERBOARD INTRODUCTION

2.1 Introduction

The IB895 is a 3.5-inch single board computer based on the Intel® Atom Cedarview chipset. The Cedar Trail is a platform that uses the Intel Cedarview-D or Cedarview -M Processor and Intel NM10 Express Chipset family in the desktop platforms.

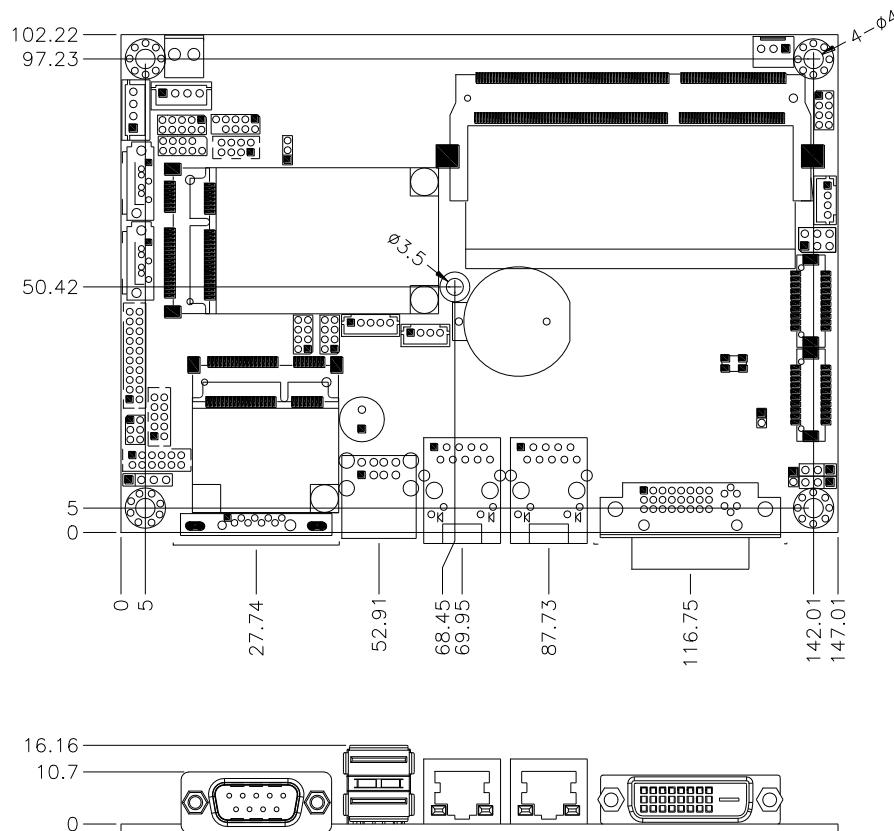
The role of the processor in the system is to manage the flow of information between the following interfaces: DDR3 System Memory interface, DVI display interface, VGA graphics interface, Low Voltage Differential Signaling (LVDS) and the Direct Media Interface (DMI). The processor supports single channel, one DDR3 SODIMMs.

The Intel® processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment. The processor is built on 32-nanometer Hi-K process technology with Micro-FCBGA11 packaging.

Specifications – Mainboard	
Model	IB895 [default silk screen model # on PCB] IB895N(N2600 onboard)
Form Factor	3.5"
CPU Type	Intel® AtomTM DC D2550 / 1MB cache / 1.86 GHz [TDP=10W] (IB895) Intel® AtomTM DC N2600 / 1MB cache / 1.60 GHz [TDP=3.5W] (IB895N) Package = FCBGA437 [22 mm x 22 mm] ; Cores / Threads = 2 / 4
Chipset	Intel® CG82NM10 PCH [TDP = 2.1W] Package = BGA360, 17mm x 17 mm
BIOS	AMI BIOS, support ACPI Function
Memory	Intel® Atom TM on-die memory controller 1x DDR3-1066 SO-DIMM socket [Horizontal type] <u>Maximum memory: 4GB for D2550; 2GB for N2600</u> Non-ECC, Unbuffered, 1.5V
LVDS	24-bit dual channel via CH7511thru eDP
VGA	Intel® GMA 3650 (Gfx freq @ 640MHz) for D2550 Intel® Graphics Media Acc GMA accelerator 3600 (Gfx freq @ 400MHz) for N2600 Supports DirectX 9 Graphics, OpenGL 3.0 DVI-I x 1 (Thru VGA + ASM1422 for DVI-D via D2550 or N2600)
LAN	Intel 82583V PCIe Gigabit LAN x 2

Audio	Intel® NM10 PCH built-in HD Audio controller + Realtek ALC269QHD Codec w/class-D speaker amplifier(2.3W per channel @ 5V power supply) [7mm x 7mm @ 48-QFN] ; support 2-channel audio out + amp
USB	NM10 built-in USB 2.0 host controller, support 6 ports
LPC I / O	Nuvoton NCT6627UD [128-pin QFP, 14x14x1.4mm] - COM #1 (RS232/422/485) support ring-in with power @500 mA (selectable for 5V or 12V) [EXAR SP339EER1 232/422/485 transceiver x 1 for jumper-less] - COM #2 (RS232 only) - COM #3 / COM #4 (RS-232 only) [Hardware Monitor] 2 x Thermal inputs; 2 x Voltage monitoring 1 x Fan Header(DC Fan type)
Serial ATA Ports	NM10 built-in SATA II controller, supports 2 ports
Expansion Slot	Mini PCI-e socket x 2 (1x Full-sized+1xHalf-sized) **Full-sized MiniPCIe(1x) support mSATA**
Digital IO	4 in & 4 out
Keyboard/ Mouse Connector	Pin headers
Edge Connector	DVI-I, 2x RJ45, 2x USB, COM1
Onboard Header/Connector	Keyboard/mouse, 4x USB 2.0, 2x DF13 for 24-bit dual channel LVDS, Audio, speaker, COM2, COM3/4, LPC (80-port card debugging purpose), 2x Mini PCI-e(1x), smart battery, backlight/brightness control, 2x power connector SATA HDD [JST type]
Watchdog Timer	Yes (256 segments, 0, 1, 2...255 sec/min)
Power Connector	+12V ~ +24V DC-in
Others	- i-Smart function (TI MSP430G2433 MCU) - AT24C02C EEPROM [SO8 type] via SMBus (Optional)
OS Support	- Windows 7 (32-bit only) - Linux
RoHS	Yes
Board Size	102mm x 147mm

Board Dimensions



2.2 Installing the Memory

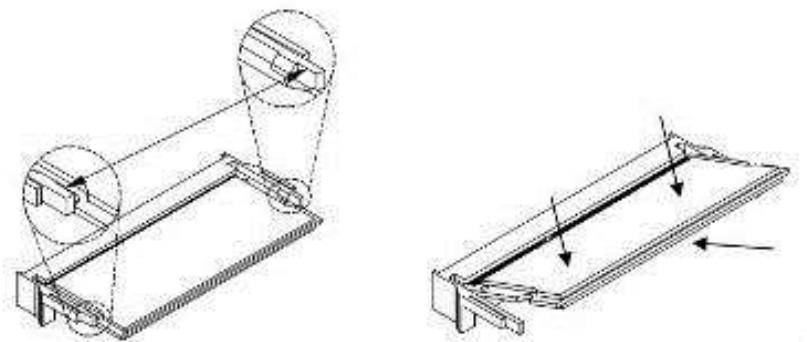
The IB895 board supports one DDR3 memory socket for a maximum total memory of 2GB or 4GB DDR3 memory type.

Note: IB895 with Intel Atom DC D2550 supports up to 4GB and IB895N with Intel Atom DC N2600 supports up to 2GB.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

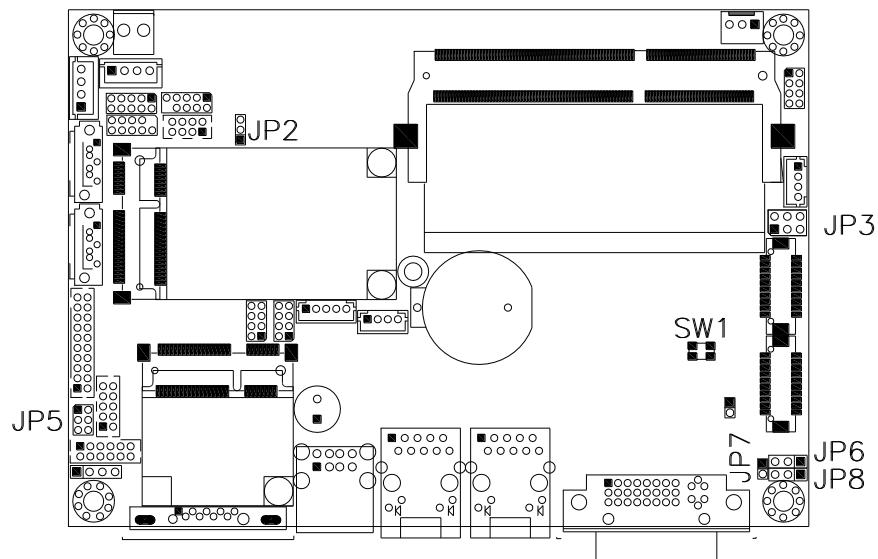
1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
3. To remove the DDR3 module, press the clips with both hands.



2.3 Setting Jumpers

Jumpers are used on IB895 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on IB895 and their respective functions.

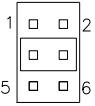
Jumper Locations on IB895



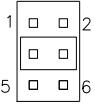
JP2: Clear CMOS Contents

JP2	Setting	Function
 1 2 3	Pin 1-2 Short/Closed	Normal
 1 2 3	Pin 2-3 Short/Closed	Clear CMOS

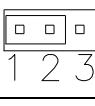
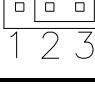
JP3: BL Voltage Setting

JP3	Setting	Function
	Pin 1-2 Short/Closed	+3.3V
	Pin 3-4 Short/Closed	+5V
	Pin 5-6 Short/Closed	+12V(Default)

JP5: COM1 RS232 RI/+5V/+12V Power Setting

JP5	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+5V

JP6: LVDS Panel Power Selection

JP6	Setting	Panel Voltage
 1 2 3	Pin 1-2 Short/Closed	3.3V (default)
 1 2 3	Pin 2-3 Short/Closed	5V

JP7: BL_ADJ_LEVEL Setting (PWM Mode)

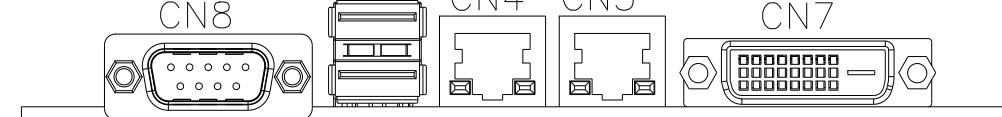
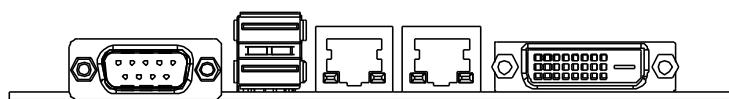
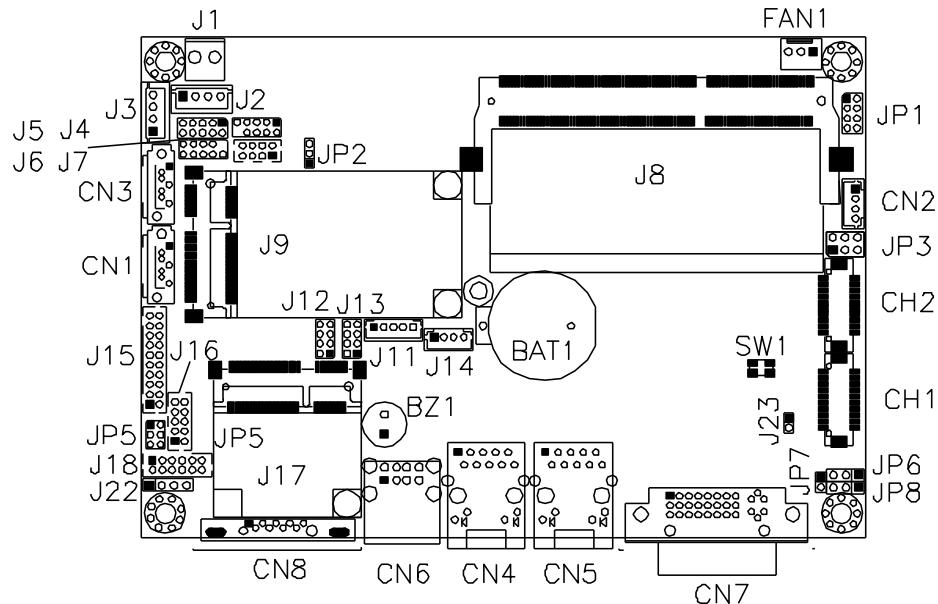
JP7	Setting	Voltage
	Open	3.3V (default)
	Close	5V

JP8: Factory use only**SW1: LVDS Panel Type Setting**

SW1-4	SW1-3	SW1-2	SW1-1	Panel Type
ON	ON	ON	ON	800*600 18bit 1ch
ON	ON	ON	OFF	1024*768 18bit 1ch
ON	ON	OFF	ON	1024*768 24bit 1ch
ON	ON	OFF	OFF	1280*768 18bit 1ch
ON	OFF	ON	ON	1280*800 18bit 1ch
ON	OFF	ON	OFF	1280*960 18bit 1ch
ON	OFF	OFF	ON	1280*1024 24bit 2ch
ON	OFF	OFF	OFF	1366*768 18bit 1ch
OFF	ON	ON	ON	1366*768 24bit 1ch
OFF	ON	ON	OFF	1440*900 24bit 2ch
OFF	ON	OFF	ON	1440*1050 24bit 2ch
OFF	ON	OFF	OFF	1600*900 24bit 2ch
OFF	OFF	ON	ON	1680*1050 24bit 2ch
OFF	OFF	ON	OFF	1600*1200 24bit 2ch
OFF	OFF	OFF	ON	1920*1080 24bit 2ch
OFF	OFF	OFF	OFF	1920*1200 24bit 2ch

2.4 Connectors

Connector Locations on IB895



CN4, CN5: Gigabit LAN (Intel 82583V)

This RJ45 LAN connector (CN4 only) features for EUP LAN wakeup.

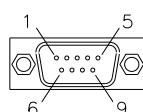
CN6: USB 1/2 Connector

CN7: VGA DVI-I Connector

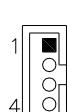
CN8: DB9 Connector

(COM1) is a DB-9 connector.

Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

COM1 is jumper-less for RS-232, RS-422 and RS-485 and configured with BIOS Selection.


Pin #	Signal Name		
	RS-232	R2-422	RS-485
1	DCD	RX+	DATA-
2	RX	RX-	DATA+
3	TX	TX+	NC
4	DTR	TX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

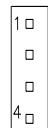
CN1, CN3: SATA Connectors**CN2: LCD Backlight Connector**


Pin #	Signal Name
1	Backlight Power
2	Backlight Enable
3	Brightness Control
4	Ground

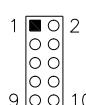
Note: Brightness Control only support PWM-Mode Panel

J1: Board Input Power Connector

Pin #	Signal Name
1	+12V to +24V
2	GND

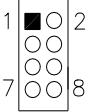
J2, J3: SATA HDD Power Connector

Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	+12V

J4: Debug 80 Port Connector (factory use only)**J5: Digital I/O Connector**

Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J6: SPI Flash Connector (factory use only)

J7: Keyboard & Mouse Connector (DF11 Connector)


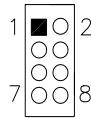
	Signal Name	Pin #	Pin #	Signal Name
1	VCC	1	2	VCC
7	MDA	3	4	KBDA
	MCL	5	6	KBCL
8	Ground	7	8	Ground

J8: DDR3 SO-DIMM Socket**J9: Mini PCIE Connector(Support mSATA)**

J9 also supports mSATA. However, when J9 is used for mSATA, then CN3 SATA port cannot be used. Only one of them can be used at one time to support SATA.

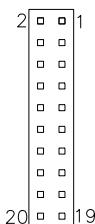
J11: Smart Battery Interface Connector


Pin #	Signal Name
1	RST
2	EXTSMI
3	Ground
4	DATA
5	CLK

J12, J13: USB3/4/5/6/7/8 Connector


	Signal Name	Pin #	Pin #	Signal Name
1	Vcc	1	2	Ground
7	D-	3	4	D+
	D+	5	6	D-
8	Ground	7	8	Vcc

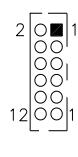
J14: MCU Flash Connector (factory use only)

J15: COM3, COM4 Serial Port (DF11 Connector)


Signal Name	Pin #	Pin #	Signal Name
DSR3	2	1	DCD3
RTS3	4	3	RXD3
CTS3	6	5	TXD3
RI3	8	7	DTR3
NC	10	9	Ground
DSR4	12	11	DCD4
RTS4	14	13	RXD4
CTS4	16	15	TXD4
RI4	18	17	DTR4
NC	20	19	Ground

J16: COM2/RS232 Serial Port

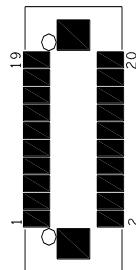
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	2	RXD, Receive data
TXD, Transmit data	3	4	DTR, Data terminal ready
GND, ground	5	6	DSR, Data set ready
RTS, Request to send	7	8	CTS, Clear to send
RI, Ring indicator	9	10	Not Used

J17: Mini PCIE Connector**J18: Audio Connector (DF11 Connector)**


Signal Name	Pin #	Pin #	Signal Name
LINEOUT_R	2	1	LINEOUT_L
Ground	4	3	JD_FRONT
LINEIN_R	6	5	LINEIN_L
Ground	8	7	JD_LINEIN
MIC-R	10	9	MIC_L
Ground	12	11	JD_MIC1

J22: Amplify Connector

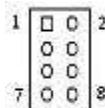

Pin #	Signal Name
1	OUTL+
2	OUTL-
3	OUTR-
4	OUTR+

J23: LVDS EEPROM Flash Connector (factory use only)**CH1, CH2: LVDS Connectors**

Signal Name	Pin #	Pin #	Signal Name
N.C	19	20	N.C
ENABLE	17	18	LCD_PWR
CLK+	15	16	CLK-
GND	13	14	GND
LD2+	11	12	LD2-
LD3+	9	10	LD3-
GND	7	8	LCD_PWR
LD1+	5	6	LD1-
GND	3	4	GND
LD0+	1	2	LD0-

JP1: Front Panel Connector

The following table shows the pin outs of the 2x4 pin header



Signal Name	Pin #	Pin #	Signal Name
Ground	1	2	PWR_SW
PWR_LED+	3	4	PWR_LED-(GND)
HDD_LED+	5	6	HDD_LED-
Ground	7	8	RESET

JP1 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. JP1 is an 8-pin header that provides interfaces for the following functions.

ATX Power ON Switch: Pins 1 and 2

This 2-pin connector is an “ATX Power Supply On/Off Switch” on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.

Power LED: Pins 3 and 4

Pin #	Signal Name
3	LED(+)
4	LED(-)

Hard Disk Drive LED Connector: Pins 5 and 6

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

Pin #	Signal Name
5	LED(+)
6	LED(-)

Reset Switch: Pins 7 and 8

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.

CHAPTER 3 BIOS SETUP

3.1 BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

3.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the key immediately allows you to enter the Setup utility. If you are a little bit late pressing the key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

Press to Enter Setup

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

System Date

Set the Date. Use Tab to switch between Data elements.

System Time

Set the Time. Use Tab to switch between Data elements.

3.3 Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Legacy OpROM Support					
Launch PXE OpROM			Disabled		
<ul style="list-style-type: none"> ▶ PCI Subsystem Settings ▶ ACPI Settings ▶ Wake up event setting ▶ CPU Configuration ▶ iSmart Configuration ▶ IDE Configuration ▶ USB Configuration ▶ W83627UHG Super IO Configuration ▶ H/W Monitor ▶ PPM Configuration 			<ul style="list-style-type: none"> → ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit 		

Launch PXE OpROM

Enable or Disable Boot Option for Legacy Network Devices.

PCI Subsystem Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Bus Driver Version	V 2.05.01				
PCI ROM Priority	Legacy ROM				
PCI Common Settings					
PCI Latency Timer	32 PCI Bus Clocks			→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit	
VGA Palette Snoop	Disabled				
PERR# Generation	Disabled				
SERR# Generation	Disabled				

PCI ROM Priority

In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop

Enables or Disables VGA Palette Registers Snooping.

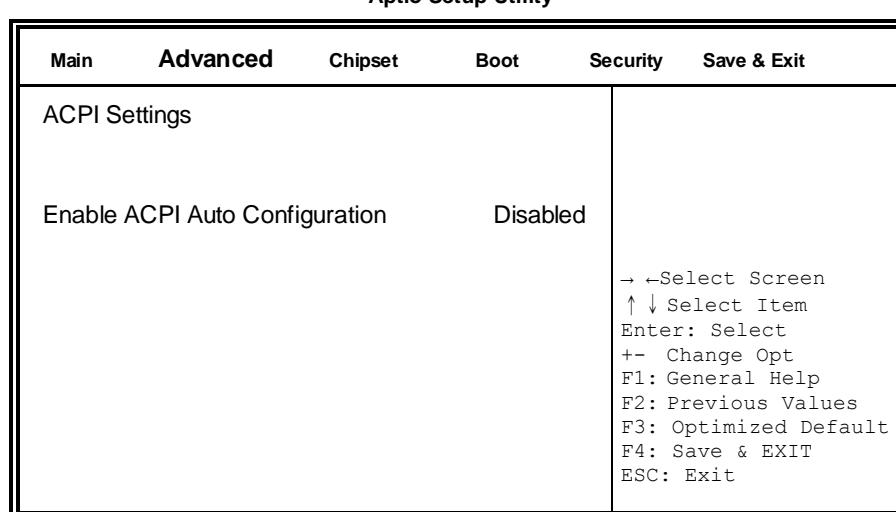
PERR# Generation

Enables or Disables PCI Device to Generate PERR#.

SERR# Generation

Enables or Disables PCI Device to Generate SERR#.

ACPI Settings



Enabled ACPI Auto Configuration

Enables or Disables BIOS ACPI Auto Configuration.

Wake up event setting

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Wake on Ring	Disabled			→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit	
Wake on PCIE PME	Disabled				

Wake on Ring

The options are Disabled and Enabled.

Wake on PCIE PME

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
CPU Configuration					
Processor Type	Intel(R) Atom(TM) CPU				
EMT64	Supported				
Processor Speed	1865 MHz				
System Bus Speed	533 MHz				
Ratio Status	14				
Actual Ratio	14				
System Bus Speed	533 MHz				
Processor Stepping	30661				
Microcode Revision	269				
L1 Cache RAM	2x56 k				
L2 Cache RAM	2x512 k				
Processor Core	Dual				
Hyper-Threading	Supported				
Hyper-Threading	Enabled				→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
Execute Disable Bit	Enabled				
Limit CPUID Maximum	Disabled				

Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Red Hat Enterprise 3 Update 3.)

Limit CPUID Maximum

Disabled for Windows XP.

iSmart Controller

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
iSmart Controller					
EuP/ErP standby power Control	Keep standby power				
Power-On after Power failure	Disable				
Schedule Slot 1	None				→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
Schedule Slot 2	None				

EuP/ErP standby power Control

Saving the power consumption on power off.

Power-On after Power failure

This field sets the system power status whether *on or off* when power returns to the system from a power failure situation.

Schedule Slot

None / Power On / Power On/Off – Setup the hour/minute for system power on

IDE Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
SATA Port0	Not Present				
SATA Port1	Not Present				
SATA Controller(s)	Enabled				→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
Configure SATA as	IDE				

SATA Controller(s)

Enable / Disable Serial ATA Controller.

Configure SATA as

- (1) IDE Mode.
- (2) AHCI Mode.

USB Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					
USB Devices:					
	None				
Legacy USB Support		Enabled			
EHCI Hand-off		Enabled			
USB hardware delays and time-outs:					
USB Transfer time-out	20 sec				→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
Device reset time-out	20 sec				
Device power-up delay	Auto				

Legacy USB Support

Enables Legacy USB support.

AUTO option disables legacy support if no USB devices are connected.

DISABLE option will keep USB devices available only for EFI applications.

EHCI Hand-off

Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

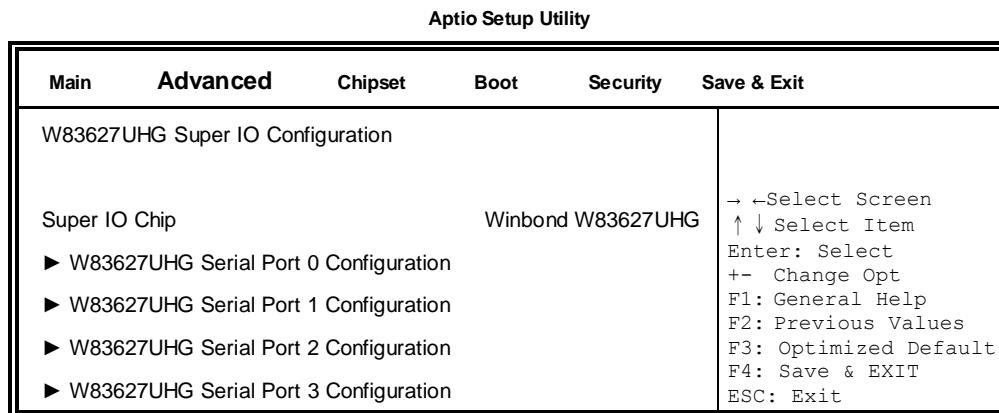
Device reset time-out

USB mass Storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. ‘Auto’ uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

Super IO Configuration



Serial Port Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

H/W Monitor

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
PC Health Status					
System temperature	+50 C				→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
CPU temperature	+55 C				
CPU Fan Speed	N/A				
VCORE	+1.184 V				
+12V	+12.032 V				
+3.3V	+3.248 V				
+5V	+4.960 V				
CPU Shutdown Temperature	Disabled				
SmartFan Control	Disabled				

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

CPU Shutdown Temperature

The default setting is Disabled.

Smart Fan Control

The options are: Disabled (default), 60 °C, 70 °C, 80 °C, 90 °C

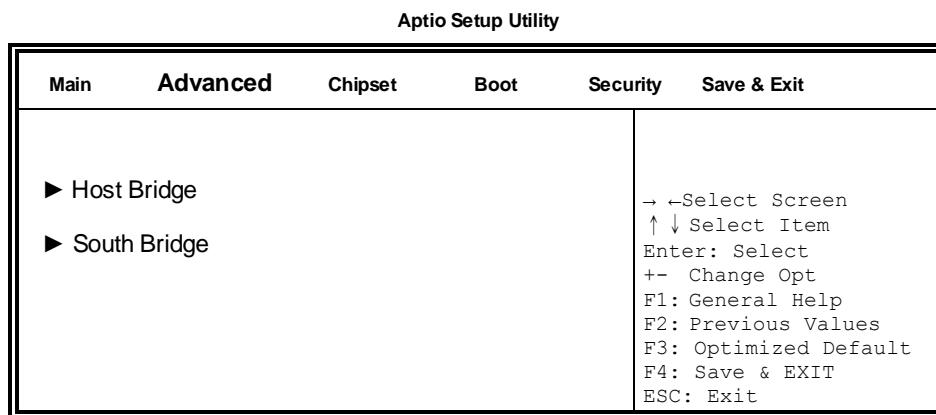
PPM Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
PPM Configuration					→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
EIST		Enabled			

3.4 Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



Host Bridge

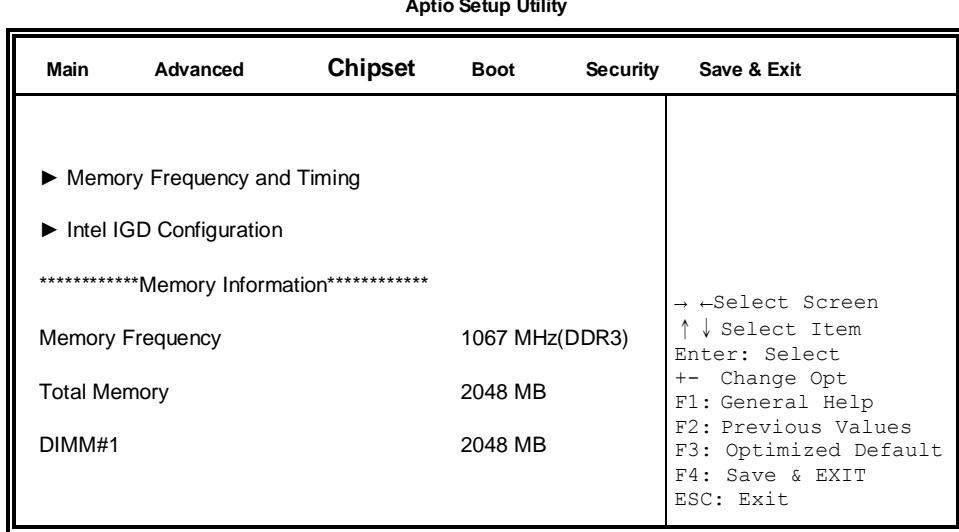
This item shows the Host Bridge Parameters.

South Bridge

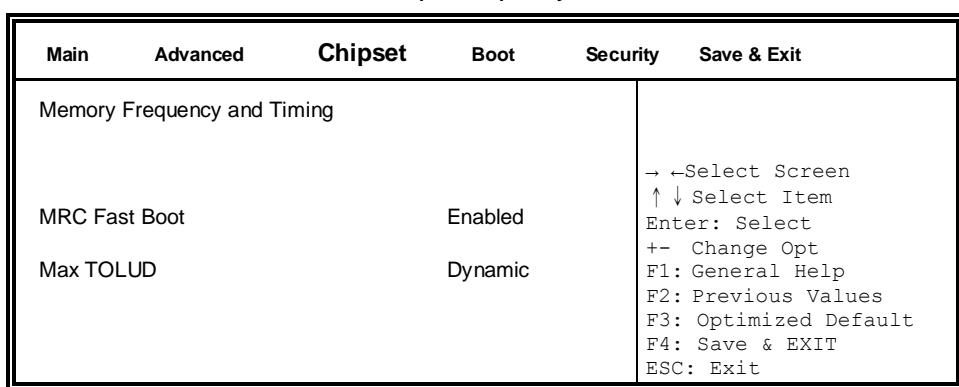
This item shows the South Bridge Parameters.

Host Bridge

This section allows you to configure the Host Bridge Chipset.



Memory Frequency and Timing



MRC Fast Boot

The options are Disabled and Enabled.

Max TOLUD

The default setting is Dynamic.

Intel IGD Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Intel IGD Configuration					→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
IGFX-Boot Type		VBIOS Default			
LVDS Back Light Control		7(MAX)			

IGFX-Boot Type

Select the video Device which will be activated during POST.

South Bridge

This section allows you to configure the South Bridge Chipset.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
► TPT Device					→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
► PCI Express Root Port0					
► PCI Express Root Port1					
► PCI Express Root Port2					
► PCI Express Root Port3					
DMI Link ASPM Control		Enabled			
PCI-Exp. High Priority Port		Disabled			
High Precision Event Timer Configuration					
High Precision Timer		Enabled			
SLP_S4 Assertion Width		1-2 Seconds			

DMI Clink ASPM Control

The control of Active State Power Management on both NB and SB side of the DMI Link.

PCI-Exp. High Priority Port

The options are Disabled, Port1, Port2, Port3, and Port4.

High Precision Event Timer Configuration

Enable/or Disable the High Precision Event Timer.

SLP_S4 Assertion Stretch Enable

Select a minimum assertion width of the SLP_S4# signal.

TPT Device

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Azalia Controller		HD Audio			
Select USB Mode		By Controllers			
UHCI #1 (port 0 and 1)		Enabled		→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit	
UHCI #2 (port 2 and 3)		Enabled			
UHCI #3 (port 4 and 5)		Enabled			
UHCI #4 (port 6 and 7)		Enabled			
USB 2.0(EHCI) Support		Enabled			

PCI Express Root Port0

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Express Port 0		Enabled			
Port 0 IOxAPIC		Disabled			
Automatic ASPM		Manual		→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit	
ASPM L0s		Root Port Only			
ASPM L1		Enabled			

PCI Express Root Port1**Aptio Setup Utility**

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Express Port 0			Auto		
Port 0 IOxAPIC			Disabled		
Automatic ASPM			Manual		
ASPM L0s			Root Port Only		
ASPM L1			Enabled		
				→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit	

PCI Express Root Port2

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Express Port 2		Auto			
Port 0 IOxAPIC		Disabled			→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
Automatic ASPM		Manual			
ASPM L0s		Disabled			
ASPM L1		Disabled			

PCI Express Root Port3

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Express Port 3		Auto			
Port 0 IOxAPIC		Disabled			→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
Automatic ASPM		Manual			
ASPM L0s		Disabled			
ASPM L1		Disabled			

Boot Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Boot Configuration					
Setup Prompt Timeout			1		
Bootup NumLock State			On		
Quiet Boot			Disabled		
Fast Boot			Disabled		
CSM16 Module Version			07.68		→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
GateA20 Active			Upon Request		
Option ROM Messages			Force BIOS		
Interrupt 19 Capture			Enabled		
CSM Support			Enabled		
Boot Option Priorities					

Setup Prompt Timeout

Number of seconds to wait for setup activation key.

65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

GateA20 Active

UPON REQUEST – GA20 can be disabled using BIOS services.

ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set display mode for Option ROM. Options: Force BIOS; Keep Current.

Interrupt 19 Capture

Enable: Allows Option ROMs to trap Int 19.

CSM Support

Enables/Disables/Auto CSM Support.

3.5 Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility						
Main	Advanced	Chipset	Boot	Security	Save & Exit	
Password Description If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights					→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit	
Administrator Password User Password						

Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

3.6 Save & Exit Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Save Changes and Exit					
Discard Changes and Exit					
Save Changes and Reset					
Discard Changes and Reset					
Save Options					→ ←Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt F1: General Help F2: Previous Values F3: Optimized Default F4: Save & EXIT ESC: Exit
Save Changes					
Discard Changes					
Restore Defaults					
Save as User Defaults					
Restore User Defaults					
Boot Override					

Save Changes and Exit

Exit system setup after saving the changes.

Discard Changes and Exit

Exit system setup without saving any changes.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Save Changes

Save Changes done so far to any of the setup options.

Discard Changes

Discard Changes done so far to any of the setup options.

Restore Defaults

Restore/Load Defaults values for all the setup options.

Save as User Defaults

Save the changes done so far as User Defaults.

Restore User Defaults

Restore the User Defaults to all the setup options.

CHAPTER 4 DRIVERS INSTALLATION

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard.

IMPORTANT NOTE:

After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

4.1 Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the disc that comes with the board. Click **Intel** and then **Intel(R) Cedarview Chipset Drivers**.



2. Click **Intel(R) Chipset Software Installation Utility**.



3. When the Welcome screen to the Intel® Chipset Device Software appears, click **Next** to continue.

4. Click **Yes** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click **Next** to continue the installation.

6. The Setup process is now complete. Click **Finish** to restart the computer and for changes to take effect.

4.2 VGA Drivers Installation

IMPORTANT NOTE: After installing the graphics driver, the default display is still LVDS. Both VGA/CRT and DVI will only be extended displays. To switch to any of these displays, use the hot key:

For VGA – **Ctrl+Alt+F1**

For DVI – **Ctrl+Alt+F3**

1. Click **Intel(R) Cedarview Graphics Driver.**



2. When the Welcome screen appears, click **Next** to continue.



3. Click **Yes** to agree with the license agreement and continue the installation.

4. On the Readme File Information screen, click **Next** to continue the installation of the Intel® Graphics Media Accelerator Driver.

5. On Setup Progress screen, click **Next** to continue.

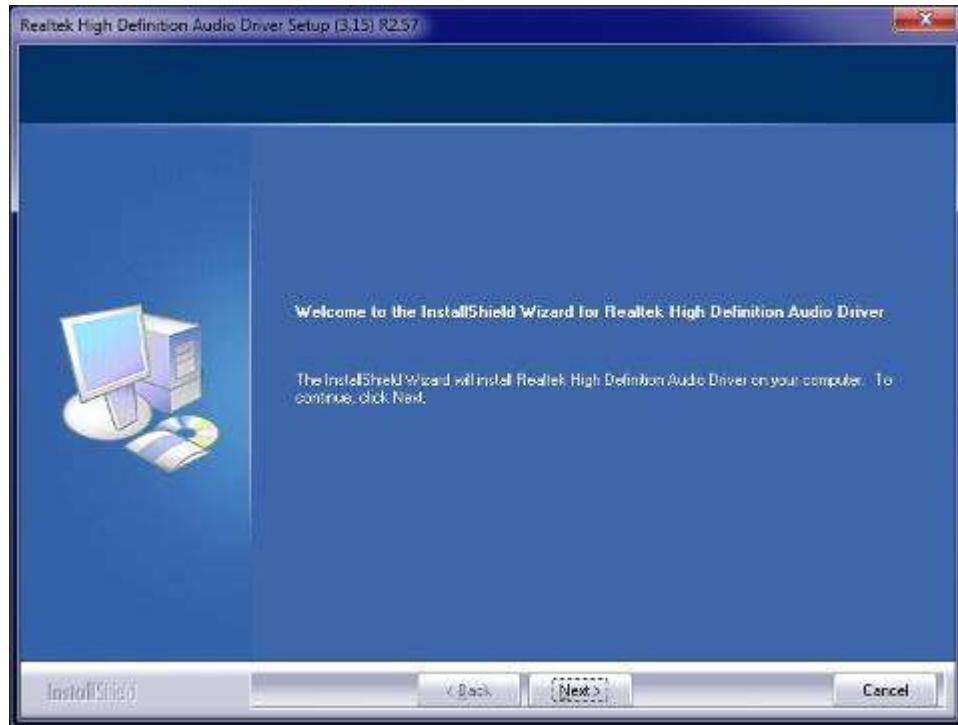
6. Setup complete. Click **Finish** to restart the computer and for changes to take effect.

4.3 Realtek HD Audio Driver Installation

1. Click **Realtek High Definition Audio Driver**.



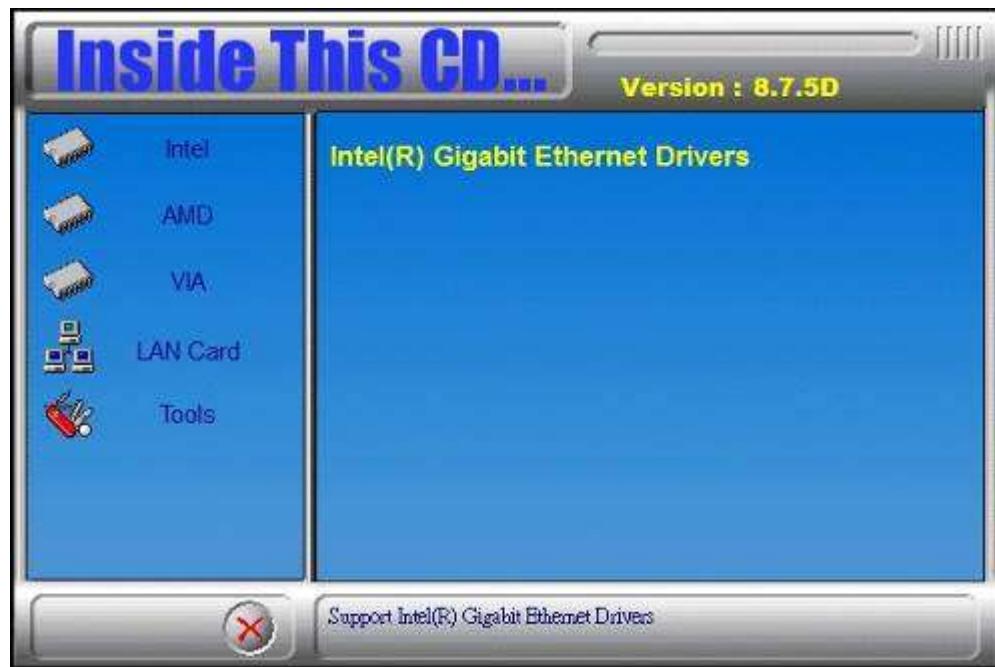
2. On the Welcome to the InstallShield Wizard screen, click **Next** to proceed with and complete the installation process.



3. Restart the computer when prompted.

4.4 LAN Drivers Installation

1. Insert the CD that comes with the board. Click **LAN Card** and then **Intel(R) LAN Controller Drivers**.
2. Click **Intel(R) Gigabit Ethernet Drivers**.



3. In the Welcome screen, click **Next**.
4. In the License Agreement screen, click **I accept the terms in license agreement** and **Next** to accept the software license agreement and proceed with the installation process.
5. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.
6. When the Ready to Install the Program screen appears, click **Install** to continue.
7. When InstallShield Wizard is complete, click **Finish**.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0000-001F	Direct memory access controller
0000-001F	PCI bus
0020-0021	Programmable interrupt controller
0024-0025	Programmable interrupt controller
0028-0029	Programmable interrupt controller
002C-002D	Programmable interrupt controller
0030-0031	Programmable interrupt controller
0034-0035	Programmable interrupt controller
0038-0039	Programmable interrupt controller
003C-003D	Programmable interrupt controller
0040-0043	System timer
0050-0053	System timer
0060-0060	Standard PS/2 Keyboard
0064-0064	Standard PS/2 Keyboard
0070-0077	System CMOS/real time clock
0081-0091	Direct memory access controller
0093-009F	Direct memory access controller
00A0-00A1	Programmable interrupt controller
00A4-00A5	Programmable interrupt controller
00A8-00A9	Programmable interrupt controller
00AC-00AD	Programmable interrupt controller
00B0-00B1	Programmable interrupt controller
00B4-00B5	Programmable interrupt controller
00B8-00B9	Programmable interrupt controller
00BC-00BD	Programmable interrupt controller
00C0-00DF	Direct memory access controller
00F0-00F0	Numeric data processor
02E8-02EF	Communications Port (COM4)
02F8-02FF	Communications Port (COM2)

Address	Device Description
03B0-03BB	Intel(R) Graphics Media Accelerator 3600 Series
03C0-03DF	Intel(R) Graphics Media Accelerator 3600 Series
03E8-03EF	Communications Port (COM3)
03F8-03FF	Communications Port (COM1)
04D0-04D1	Programmable interrupt controller
0D00-FFFF	PCI bus
D000-DFFF	Intel(R) N10/ICH7 Family PCI Express Root Port - 27D2
E000-EFFF	Intel(R) N10/ICH7 Family PCI Express Root Port - 27D0
F000-F01F	Intel(R) N10/ICH7 Family SMBus Controller - 27DA
F020-F03F	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CB
F040-F05F	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CA
F060-F07F	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C9
F080-F09F	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C8
F0A0-F0AF	Intel(R) N10/ICH7 Family Serial ATA Storage Controller - 27C0
F0B0-F0B3	Intel(R) N10/ICH7 Family Serial ATA Storage Controller - 27C0
F0C0-F0C7	Intel(R) N10/ICH7 Family Serial ATA Storage Controller - 27C0
F0D0-F0D3	Intel(R) N10/ICH7 Family Serial ATA Storage Controller - 27C0
F0E0-F0E7	Intel(R) N10/ICH7 Family Serial ATA Storage Controller - 27C0
F0F0-F0F7	Intel(R) Graphics Media Accelerator 3600 Series

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices.

Level	Function
IRQ 0	System timer
IRQ 1	Standard PS/2 Keyboard
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 5	Communications Port (COM3)
IRQ 7	Communications Port (COM4)
IRQ 8	System CMOS/real time clock
IRQ 11	Intel(R) N10/ICH7 Family SMBus Controller - 27DA
IRQ 12	Microsoft PS/2 Mouse
IRQ 13	Numeric data processor
IRQ 16	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CB
IRQ 18	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CA
IRQ 19	Intel(R) N10/ICH7 Family Serial ATA Storage Controller - 27C0
IRQ 19	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C9
IRQ 22	High Definition Audio Controller
IRQ 23	Intel(R) N10/ICH7 Family USB2 Enhanced Host Controller - 27CC
IRQ 23	Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C8
IRQ 4294967290	Intel(R) 82583V Gigabit Network Connection
IRQ 4294967291	Intel(R) 82583V Gigabit Network Connection #2
IRQ 4294967292	Intel(R) Graphics Media Accelerator 3600 Series
IRQ 4294967293	Intel(R) N10/ICH7 Family PCI Express Root Port - 27D2
IRQ 4294967294	Intel(R) N10/ICH7 Family PCI Express Root Port - 27D0

C. Digital I/O Sample Code

File of the W627UHG.H

```
//-----
//  

// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY  

// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE  

// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  

// PURPOSE.  

//  

//-----  

#ifndef __W627UHG_H  

#define __W627UHG_H 1  

//-----  

#define W627UHG_INDEX_PORT (W627UHG_BASE)  

#define W627UHG_DATA_PORT (W627UHG_BASE+1)  

//-----  

#define W627UHG_REG_LD 0x07  

//-----  

#define W627UHG_UNLOCK 0x87  

#define W627UHG_LOCK 0xAA  

//-----  

unsigned int Init_W627UHG(void);  

void Set_W627UHG_LD( unsigned char);  

void Set_W627UHG_Reg( unsigned char, unsigned char);  

unsigned char Get_W627UHG_Reg( unsigned char);  

//-----  

#endif //__W627UHG_H
```

```
File of the W627UHG.CPP

//-----
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.

//-----
#include "W627UHG.H"
#include <dos.h>
//-----

unsigned int W627UHG_BASE;
void Unlock_W627UHG (void);
void Lock_W627UHG (void);
//-----

unsigned int Init_W627UHG(void)
{
    unsigned int result;
    unsigned char ucDid;

    W627UHG_BASE = 0x4E;
    result = W627UHG_BASE;

    ucDid = Get_W627UHG_Reg(0x20);
    if (ucDid == 0xA2)                                //W83627UHG??
    {
        goto Init_Finish;    }

    W627UHG_BASE = 0x2E;
    result = W627UHG_BASE;

    ucDid = Get_W627UHG_Reg(0x20);
    if (ucDid == 0xA2)                                //W83627UHG??
    {
        goto Init_Finish;    }

    W627UHG_BASE = 0x00;
    result = W627UHG_BASE;
```

```
Init_Finish:  
    return (result);  
}  
//-----  
void Unlock_W627UHG (void)  
{  
    outportb(W627UHG_INDEX_PORT, W627UHG_UNLOCK);  
    outportb(W627UHG_INDEX_PORT, W627UHG_UNLOCK);  
}  
//-----  
void Lock_W627UHG (void)  
{  
    outportb(W627UHG_INDEX_PORT, W627UHG_LOCK);  
}  
//-----  
void Set_W627UHG_LD( unsigned char LD)
```

```
{  
    Unlock_W627UHG();  
    outportb(W627UHG_INDEX_PORT, W627UHG_REG_LD);  
    outportb(W627UHG_DATA_PORT, LD);  
    Lock_W627UHG();  
}  
//-----  
void Set_W627UHG_Reg( unsigned char REG, unsigned char DATA)  
{  
    Unlock_W627UHG();  
    outportb(W627UHG_INDEX_PORT, REG);  
    outportb(W627UHG_DATA_PORT, DATA);  
    Lock_W627UHG();  
}  
//-----  
unsigned char Get_W627UHG_Reg(unsigned char REG)  
{  
    unsigned char Result;  
    Unlock_W627UHG();  
    outportb(W627UHG_INDEX_PORT, REG);  
    Result = inportb(W627UHG_DATA_PORT);  
    Lock_W627UHG();  
    return Result;  
}  
//-----
```

File of the MAIN.CPP

```

//-----
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.

//-----
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "W627UHG.H"
//-----

int main (void);

void Dio5Initial(void);
void Dio5SetOutput(unsigned char);
unsigned char Dio5GetInput(void);
void Dio5SetDirection(unsigned char);
unsigned char Dio5GetDirection(void);
//-----

int main (void)
{
    char SIO;

    SIO = Init_W627UHG();
    if (SIO == 0)
    {
        printf("Can not detect Winbond 83627UHG, program abort.\n");
        return(1);
    }

    Dio5Initial();

    //for GPIO50..57
    Dio5SetDirection(0x0F); //GP50..53 = input, GP54..57=output

```

```
printf("Current DIO direction = 0x%X\n", Dio5GetDirection());  
  
printf("Current DIO status = 0x%X\n", Dio5GetInput());  
  
printf("Set DIO output to high\n");  
Dio5SetOutput(0x0F);  
  
printf("Set DIO output to low\n");  
Dio5SetOutput(0x00);  
  
return 0;
```

```

}

//-----
void Dio5Initial(void)
{
    unsigned char ucBuf;

    Set_W627UHG_LD(0x08);                                //switch to logic device 8
    //enable the GP5 group
    ucBuf = Get_W627UHG_Reg(0x30);
    ucBuf |= 0x02;
    Set_W627UHG_Reg(0x30, ucBuf);

}

//-----
void Dio5SetOutput(unsigned char NewData)
{
    Set_W627UHG_LD(0x08);                                //switch to logic device 8
    Set_W627UHG_Reg(0xE1, NewData);

}

//-----
unsigned char Dio5GetInput(void)
{
    unsigned char result;

    Set_W627UHG_LD(0x08);                                //switch to logic device 8
    result = Get_W627UHG_Reg(0xE1);
    return (result);

}

//-----
void Dio5SetDirection(unsigned char NewData)
{
    //NewData : 1 for input, 0 for output
    Set_W627UHG_LD(0x08);                                //switch to logic device 8
    Set_W627UHG_Reg(0xE0, NewData);

}

//-----
unsigned char Dio5GetDirection(void)
{
    unsigned char result;
}

```

```
Set_W627UHG_LD(0x08); //switch to logic device 8
result = Get_W627UHG_Reg(0xE0);
return (result);
}
//-----
```

D. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

File of the W627UHG.CPP

```
//-----
//  

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// PURPOSE.  

//  

//-----  

#include "W627UHG.H"  

#include <dos.h>  

//-----  

unsigned int W627UHG_BASE;  

void Unlock_W627UHG (void);  

void Lock_W627UHG (void);  

//-----  

unsigned int Init_W627UHG(void)  

{  

    unsigned int result;  

    unsigned char ucDid;  

    W627UHG_BASE = 0x4E;  

    result = W627UHG_BASE;  

    ucDid = Get_W627UHG_Reg(0x20);  

    if (ucDid == 0xA2)                                //W83627UHG??  

    {  goto Init_Finish;  }
```

```
W627UHG_BASE = 0x2E;  
result = W627UHG_BASE;  
  
ucDid = Get_W627UHG_Reg(0x20);  
if (ucDid == 0xA2)                                //W83627UHG??  
{    goto Init_Finish;  }  
  
W627UHG_BASE = 0x00;  
result = W627UHG_BASE;
```

```

Init_Finish:
    return (result);
}

//-----
void Unlock_W627UHG (void)
{
    outportb(W627UHG_INDEX_PORT, W627UHG_UNLOCK);
    outportb(W627UHG_INDEX_PORT, W627UHG_UNLOCK);
}

//-----
void Lock_W627UHG (void)
{
    outportb(W627UHG_INDEX_PORT, W627UHG_LOCK);
}

//-----
void Set_W627UHG_LD( unsigned char LD)
{
    Unlock_W627UHG();
    outportb(W627UHG_INDEX_PORT, W627UHG_REG_LD);
    outportb(W627UHG_DATA_PORT, LD);
    Lock_W627UHG();
}

//-----
void Set_W627UHG_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_W627UHG();
    outportb(W627UHG_INDEX_PORT, REG);
    outportb(W627UHG_DATA_PORT, DATA);
    Lock_W627UHG();
}

//-----
unsigned char Get_W627UHG_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_W627UHG();
    outportb(W627UHG_INDEX_PORT, REG);
    Result = inportb(W627UHG_DATA_PORT);
    Lock_W627UHG();
}

```

```
    return Result;  
}  
//----------------------------------------------------------------------------
```

File of the W627UHG.H

```
//-----  
//  
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// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  
// PURPOSE.  
//  
//-----  
#ifndef __W627UHG_H  
#define __W627UHG_H 1  
//-----  
#define W627UHG_INDEX_PORT (W627UHG_BASE)  
#define W627UHG_DATA_PORT (W627UHG_BASE+1)  
//-----  
#define W627UHG_REG_LD 0x07  
//-----  
#define W627UHG_UNLOCK 0x87  
#define W627UHG_LOCK 0xAA  
//-----  
unsigned int Init_W627UHG(void);  
void Set_W627UHG_LD( unsigned char);  
void Set_W627UHG_Reg( unsigned char, unsigned char);  
unsigned char Get_W627UHG_Reg( unsigned char);  
//-----  
#endif //__W627UHG_H
```

File of the MAIN.CPP

```

//-----
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// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.

//-----
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "W627UHG.H"
//-----

int main (void);

void WDTInitial(void);
void WDTEnable(unsigned char);
void WDTDDisable(void);

//-----
int main (void)
{
    char SIO;

    SIO = Init_W627UHG();
    if (SIO == 0)
    {
        ..... printf("Can not detect Winbond 83627UHG, program abort.\n");
        ..... return(1);
    }

    WDTInitial();

    WDTEnable(10);

    WDTDDisable();
}

```

```
    return 0;
}

//-----
void WDTInitial(void)
{
    unsigned char bBuf;
    Set_W627UHG_LD(0x08); .....//switch to logic device 8
    bBuf = Get_W627UHG_Reg(0x30);
    bBuf &= (~0x01);
    Set_W627UHG_Reg(0x30, bBuf); .....//Enable WDTO
}
//-----
void WDTEnable(unsigned char NewInterval)
```

```
{  
    unsigned char bBuf;  
  
    Set_W627UHG_LD(0x08); .....//switch to logic device 8  
    Set_W627UHG_Reg(0x30, 0x01);..... //enable timer  
    bBuf = Get_W627UHG_Reg(0xF5);  
    bBuf &= (~0x08);  
    Set_W627UHG_Reg(0xF5, bBuf); .....//count mode is second  
  
    Set_W627UHG_Reg(0xF6, NewInterval); .....//set timer  
}  
//-----  
void WDTDisable(void)  
{  
    Set_W627UHG_LD(0x08); .....  
    Set_W627UHG_Reg(0xF6, 0x00);..... //clear watchdog timer  
    Set_W627UHG_Reg(0x30, 0x00);.....//watchdog disabled  
}  
//-----
```